first and second sections having first and second doping concentration gradients, respectively, the first section extending a first vertical distance below the source and having a lowest doping concentration nearest the source and a highest doping concentration farthest from the source, the second section being disposed beneath the first section and having a lowest doping concentration nearest the first section and a highest doping concentration farthest from the first section, the highest doping concentration of the first section being substantially the same as the lowest doping concentration of the second section, the source having a doping concentration greater than the lowest doping concentration of the first section; and

first and second field plate members respectively disposed on opposite sides of the drift region, each of the field plate members being respectively insulated from the first and second sidewalls of the mesa by a dielectric material, the first and second field plate members also being insulated from the substrate, the first and second field plate members extending in the vertical direction from adjacent the upper portion to adjacent the bottom portion of the mesa.

2. The power transistor of claim **1** wherein the first and second doping concentration gradients are each substantially linear.

3. The power transistor of claim **1** wherein the second doping concentration gradient is at least 10% higher that the first doping concentration gradient.

4. The power transistor of claim **1** wherein the drift region further comprises a third section, the third section being disposed beneath the second section and having a lowest doping concentration nearest the second section and a highest doping concentration farthest from the second section, the highest doping concentration of the second section being substantially the same as the lowest doping concentration of the third section.

5. The power transistor of claim **1** wherein the drift region comprises an epitaxial layer formed over the substrate.

6. The power transistor of claim **1** further comprising a drain electrode formed on a bottom surface of the substrate, the drain electrode being electrically connected to the drain.

7. The power transistor of claim **1** further comprising a source electrode electrically connected to the source.

8. The power transistor of claim **7** wherein the source electrode is also electrically connected to the first and second field plates.

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